TMA: HIGH SPEED DIGITAL SIGNAL INTEGRITY

Date & Time: Monday, June 12, 8:00 AM – 5:00 PM
Location:

Topics & Speakers:

→ Overview of High Speed Digital Systems and the Key Issues Facing Today's Designers, **Mike Resso,** Agilent Technologies, USA

→ Development of Gb/s CMOS Equalization Solutions, **Joy Laskar,** Georgia Tech., USA

→ Channel Modeling for 10 GB Ethernet over Copper Technologies, **Anh-Vu Pham,** UC Davis, USA

→ Advanced Package Design Validation Methods Using a High-Resolution TDR and a Commercially Available High-Speed Chip, **Dong Ho-Han,** Intel, USA

→ Accurate Calibration and Measurement of Non-Insertable Fixture in FPGA and ASIC Device Characterization, **Hong Shi,** Altera**,** USA

→ S-parameter characterization of operational transmitters and channels in digital communications systems, **Greg LeCheminant,** Agilent**,** USA

→ The State of IEEE 802.3ap Backplane Ethernet, **John D'Ambrosia,** Tyco, USA

→ Practical Design Considerations for 10 to 25 Gbps Backplane Copper Serial Links, **Ravi Kollipara,** Rambus, USA

→ Opening Closed Eyes: Analysis and Equalization of High-Data-Rate Signals on Buses and Backplanes, **Ransom Stephens, PhD.**, Teraspeed Consulting Group, USA

Organizers:
Tom Ruttan, Intel Corp.
Mike Resso, Agilent Technologies

Sponsors: 67th ARFTG Conference
MTT-11 Microwave Measurements
MTT-12 Microwave and Millimeter-Wave Packaging and Manufacturing

Topics Level: Tutorial

This full day signal integrity workshop will address high speed signal integrity design, modelling and measurement for computer and communication systems. Advanced tools are now required to validate compliance to data transmission including differential insertion loss, mixed mode analysis and eye diagram analysis. New and innovative techniques will be discussed in multiple technical papers by a wide variety of experts. Learn the latest development techniques to achieve your design and time to market goals.

The participants in this workshop will be exposed to an overview of computer backplane architecture and design to familiarize the MTT attendees with this topic, the language of high speed digital design, the meaning of signal integrity, frequency domain and time domain measurement techniques, modelling tools and best design practices.

Topics covered by the presentations will include the following:

- Overview of High Speed Digital Systems and the Key Issues Facing Today's Designers.
- Modelling techniques for high speed channels
- Design concepts and techniques for digital board level systems
- Frequency and time domain measurement methods and results
- The State of IEEE 802.3ap Backplane Ethernet
- New techniques for improving high speed digital interconnect performance