



## **Multiport / Differential Measurements for Signal Integrity Workshop**

72<sup>th</sup> ARFTG, FALL 2008, Friday Dec. 12 1:15 PM – 5:00 PM, Portland, OR

The signal integrity workshop addresses the challenging issues of high speed passive interconnect design and characterization. Several topics will be covered, ranging from crosstalk characterization of Multi-Gigabit BGA packaging to multiport VNA use and applications for backplane analysis and model validation using a new error vector magnitude technique. The specific case of differential signals is discussed and a noise modelling technique for differential circuits is proposed.

### **Scheduled Speakers:**

1:15pm – 1:55pm	Valeria Teppati – Politecnico di Torino
1:55pm – 2:35pm	Matthew Claudius – Intel,
2:35pm – 3:15pm	Heidi Barnes – Verigy,
3:15pm – 3:40pm	Coffee break,
3:40pm – 4:20pm	Jack Carrel – Xilinx,
4:20pm – 5:00pm	Julien Lintignat – XLIM University of Limoges.

**Organizers:** Mike Resso, Agilent Technologies  
Ali Boudiaf, Focus Microwaves

### **Multiport and mixed-mode measurements**

Valeria Teppati, Andrea Ferrero

**Abstract:** Multiport S-parameter measurements are increasing in importance due to the higher and higher processors speed. Moreover, differential transmission lines and devices are widely used for their characteristics of immunity to disturbances. In this talk, the most common multiport VNA architectures and their calibration models and techniques will be described. A recently introduced error model for partial reflectometer VNA architectures will be shown. Finally, some general validity rules for choosing successful multiport standard sequences will be revised.

**Valeria Teppati** received the electronic engineering degree in electronics and the Ph.D. degree in electronic instrumentation from Politecnico di Torino, Italy, in 1999 and 2003 respectively. Since 2003 she has worked at the Department of Electronics as a research and teaching assistant. In 2005 she became an Assistant Professor. Her research interests involve linear and non-linear microwave measurement techniques, uncertainty evaluation and reduction, multiport measurements.

## **Model-to-Measurement Correlation Through Automated Error Vector Magnitude Calculation**

Matthew Claudius

**Abstract:** This paper describes the development of a quantitative and objective technique for comparing scattering parameters of simulation models and measurements based on Error Vector Magnitude (EVM). A discussion of some current correlation methods and their limitations is followed by an introduction to EVM and its use as a quantitative and objective correlation method. Next, the implementation of this method into an automated analysis tool is discussed. Finally, results illustrating the EVM method applied to model-to-measurement correlation of multiport (2, 4, 8, & 12-port) s-parameter data is demonstrated.

**Matthew Claudius** obtained his degree from Vanderbilt University in 2000, and began his career at Intel's Test Tooling Operation where he worked in probecard design. In ITTO, he built high-frequency models for PCBs and multi-layer ceramics, developing Intel's first full-path probecard models validated by VNA measurement. Now, Matt is a Sr. Electrical Analysis Engineer on the technical pathfinding team in Intel's Sort Test Technology Development department, focusing on signal integrity for the past 7 years. He develops test hardware solutions for Intel chips that are generally 4-6 years away from production. Additionally, Matt works on increasing his team's modeling and simulation capability. Currently, his primary role involves increasing simulation confidence through objective frequency-domain model correlation techniques (such as error vector magnitude calculation) and developing methods by which models can be correlated to measurements in their end-use environment.

## **Crosstalk at the BGA Ball-Out Presents Significant Challenges for Multi-Gigabit ATE At-Speed Testing**

Heidi Barnes

**Abstract:** Silicon I/O cell densities on complex graphics and microprocessor integrated circuits easily require over 100 channels of differential pairs running in parallel with each other. Designing a BGA ballout with the correct Ground-Signal topology to insure signal integrity at 5Gbps data rates and beyond will require the control of crosstalk as the ballout pitch continues to decrease and the density of I/Os go up. Verifying that a part meets an acceptable level of crosstalk on all of the I/Os for the end user application is not a simple task for the ATE test engineer. A close look at the selection of reference planes and the topology used to test a high speed I/O device will show how this can change the crosstalk behavior and make it difficult for de-embedding. The concept of "in-situ" ATE testing will be

proposed for more closely replicating the BGA via field of an end-user application and thus get closer to verifying the true "at-speed" performance.

**Heidi Barnes** is a senior application consultant for high frequency device interface board designs on Verigy's V93000 semiconductor test system focusing on both digital and analog controlled impedance transitions for full path signal integrity. Prior to this she was with the Agilent's Microwave Technology Center working with thin film, thick film, PCB laminate chip and wire, and machined metal packaging technologies for DC to 20 GHz analog and digital applications. She joined Agilent Technologies (now Verigy) in 1997 and holds a Bachelor of Science degree in electrical engineering from the California Institute of Technology.

## **Utilizing 12-port s-parameters for Backplane Analysis**

Jack Carrel

**Abstract:** The telecommunications market demands high speed routers and switches that provide virtually instantaneous bandwidth. The answer for this demand is backplanes with many multi-gigabit serial channels. Designing, building, and characterizing these backplanes is becoming more challenging with every increase in the serial bit rate. A network equipment manufacturer company's whole product line depends on the longevity of the backplane. Upgrade and innovation are implemented with daughter cards, but the backplane is the anchor that holds the customer base. Because of this, backplanes have to be designed and built to last often through several line card product generations. There are 3 commonly used tools for characterizing multi-gigabit interconnect channels, the TDR, the VNA, and the Eye diagram. The latest tool in the test and measurement world is the 12-port Vector Network Analyzer. This paper will show how to make tough design decisions for the physical layer using 12-port s-parameters as the guiding criteria.

**Jack Carrel** is a System IO Specialist at Xilinx. He has over 25 years of experience in product development and design in the fields of Instrumentation, Test and Measurement, and Telecommunications. His background includes development of electro-optic modules, Multi-gigabit transceiver boards, high speed and high resolution data acquisition systems for government and commercial applications. Most recently he has been involved in product design using multi-gigabit transceivers with specific focus on PCB design issues. He has published in several professional publications. Jack received his Bachelor of Science degree in Electrical Engineering from the University of Oklahoma.

## **Analysis and characterization of differential RF devices**

Julien Lintignat

**Abstract:** The need for take into account the signal integrity in multiport devices becomes more and more insistent. This presentation describes the principle of design and characterization for differential

circuits. First the background and the main characteristics of differential systems is presented. Then some discussions about noise figure and signal to noise ratio are addressed. Finally, good practices of RF design and characterization that could be used for high speed digital interconnects are depicted.

**Julien Lintignat** was born in Saint Maurice, France on 1979. He received his master and Ph.D. degrees in High-Frequencies and Optical Telecommunications from the University of Limoges, France, in 2003 and 2006, respectively. He is currently Assistant Professor at the University of Limoges in the C<sup>2</sup>S<sup>2</sup> department of the XLIM research institute. His research interests are the analysis, design, development and measurement of RF and microwave differential devices, circuits and systems.