Pulse Profiling for AlGaN/GaN HEMTs Large Signal Characterizations

Jad FARAJ

Outline

Motivations for LSNA Load-Pull Measurements Pulse Profiling

The LSNA

Pulse Profile Mode of LSNA Load-PULL

The Pulsed and Pulse Profiling Measurement Results

Conclusions and Perspectives

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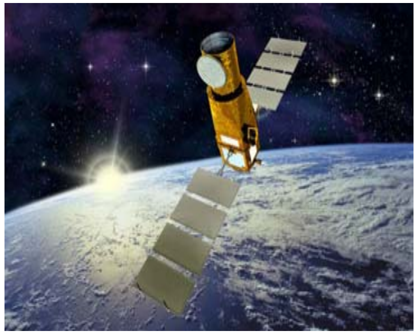

- Key factors in power amplifiers
  - Linearity
  - Gain
  - Power Efficiency

- Tendencies:
  - New devices (GaN)
  - New designs (Switched amplifiers)
  - New requirements (High power, Wideband modulations)

- Designer's nightmares:
  - Memory effects : Thermal effects, Traps
  - Reliability
  - Poor models

- Rescue solutions:
  - Device Measurements
  - Circuit Measurements
  - Comparison with simulation results

- Time Domain Load-Pull setups can measure the drain load line of devices up to very high power

- But… more and more high power devices are used in pulsed mode, or with very high peak to average ratios

- The memory effects are more and more to be accurately considered, in particular the shift of characteristics

- RF designers can take benefits of transient envelope simulators. But once again, such simulations have to be checked with measurements

We will propose a measurement system with the capability to perform pulse profiling of time domain measurements

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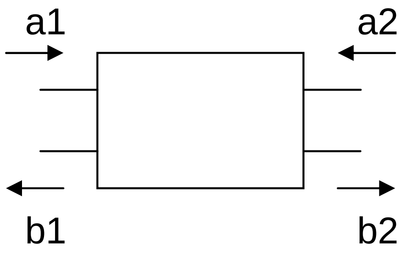
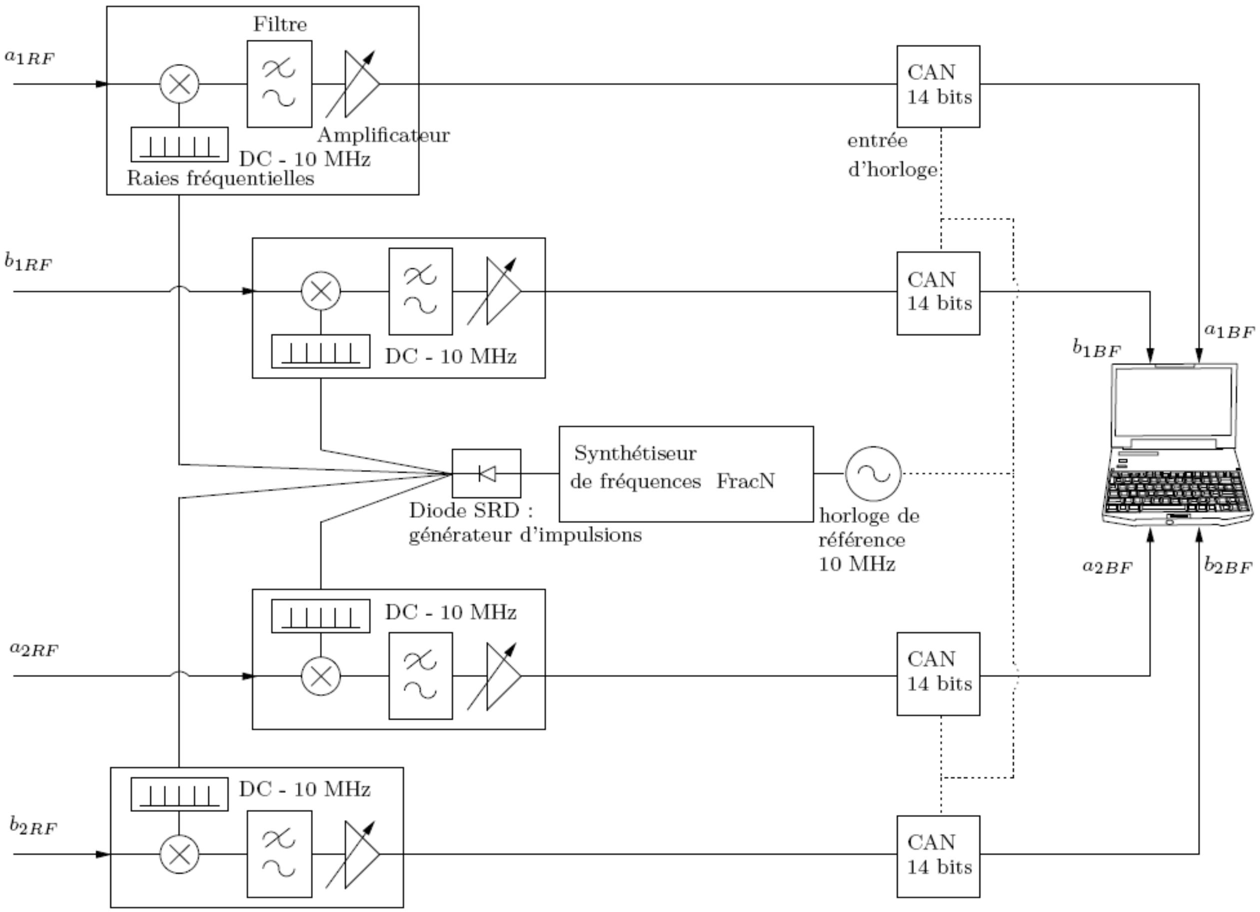
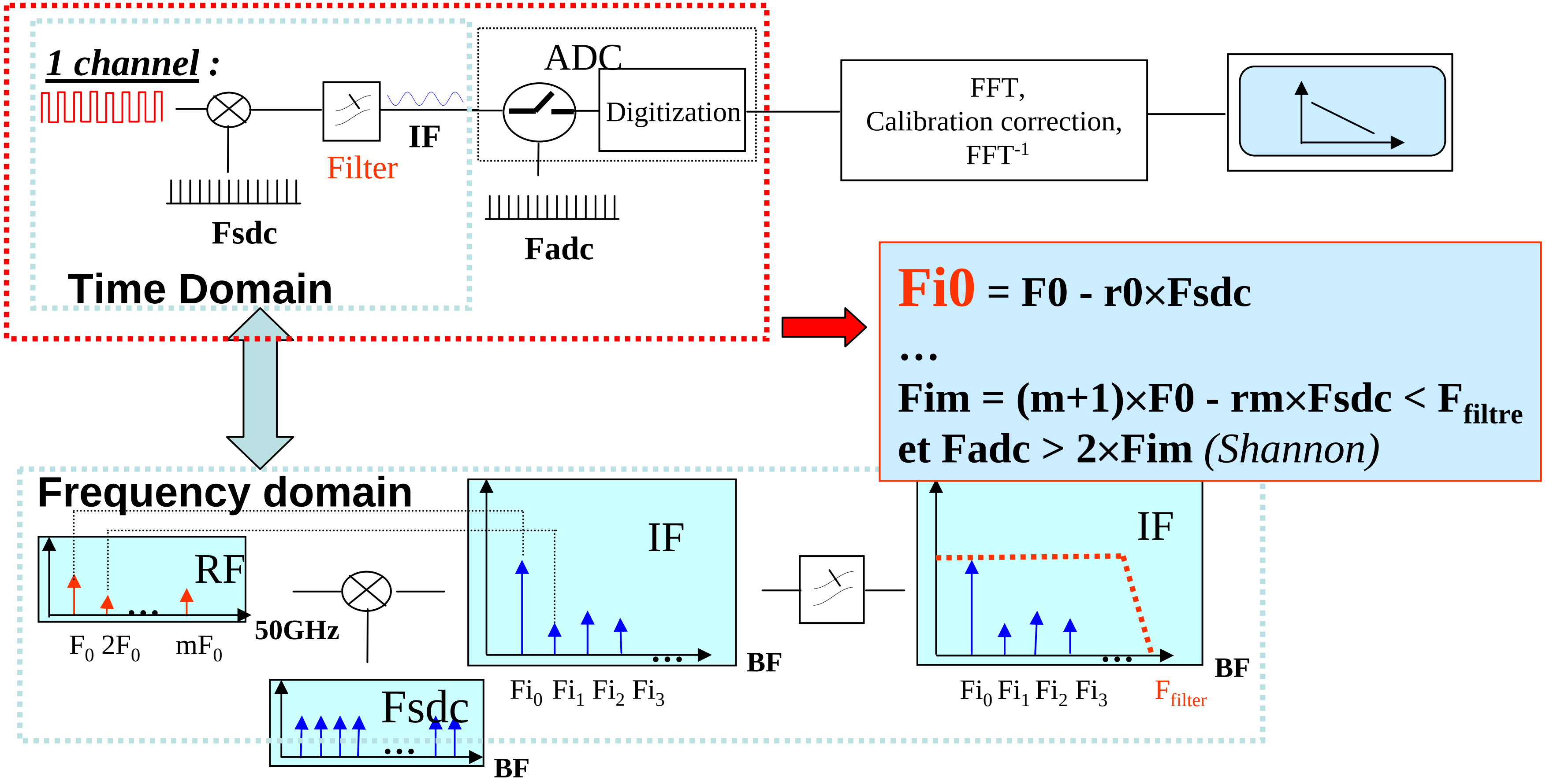




A 4 paths and 4 samplers system

The LSNA in CW Mode



$Fi0 = F0 - r0 \times Fsdc$

…

$Fim = (m+1) \times F0 - rm \times Fsdc < F_{filtre}$

et $Fadc > 2 \times Fim$ *(Shannon)*

All the frequency components of interest are simultaneously available in the IF domain

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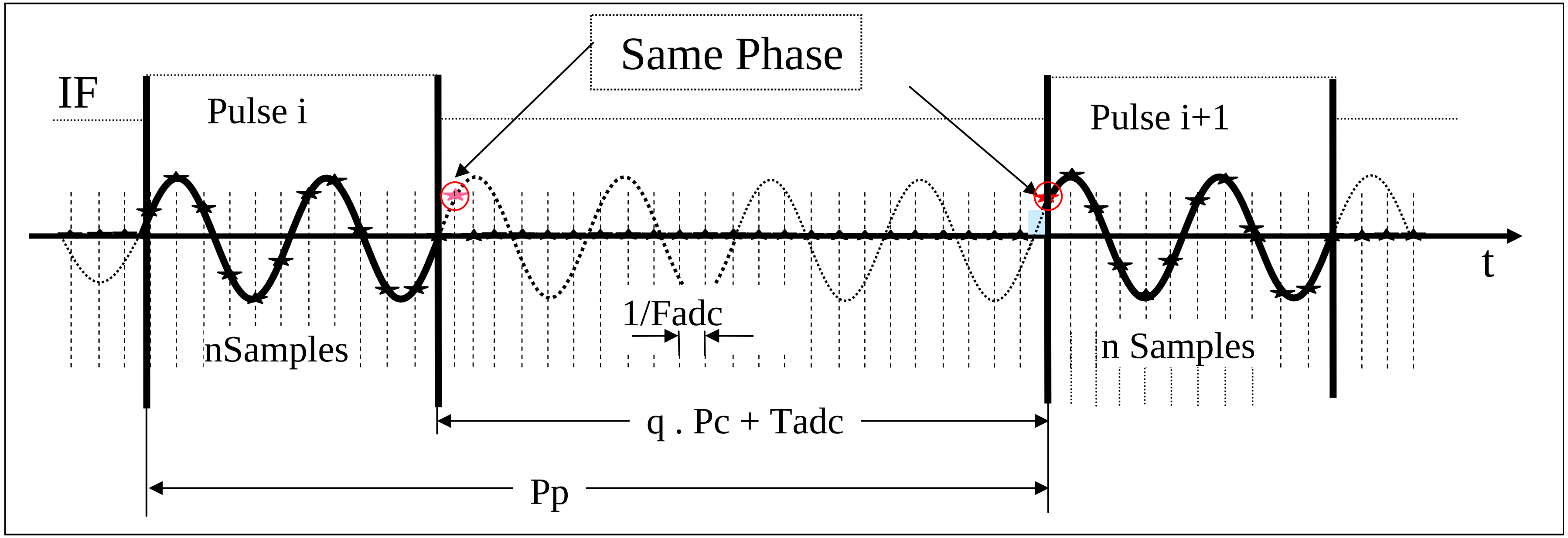


⇔ Two mathematical relationships:

- *a common period between F0, Fsdc, Fadc noted Pc*
- *a* relationship between the common period Pc and the Pulses period (Pp) $\Rightarrow \; Pp = q \times Pc + (n-1) \times Tadc + Tadc$

A synchronized pulsed mode without dynamical losses

- The Same conditions for CW mode (F0,,,,,,,,,,mF0):

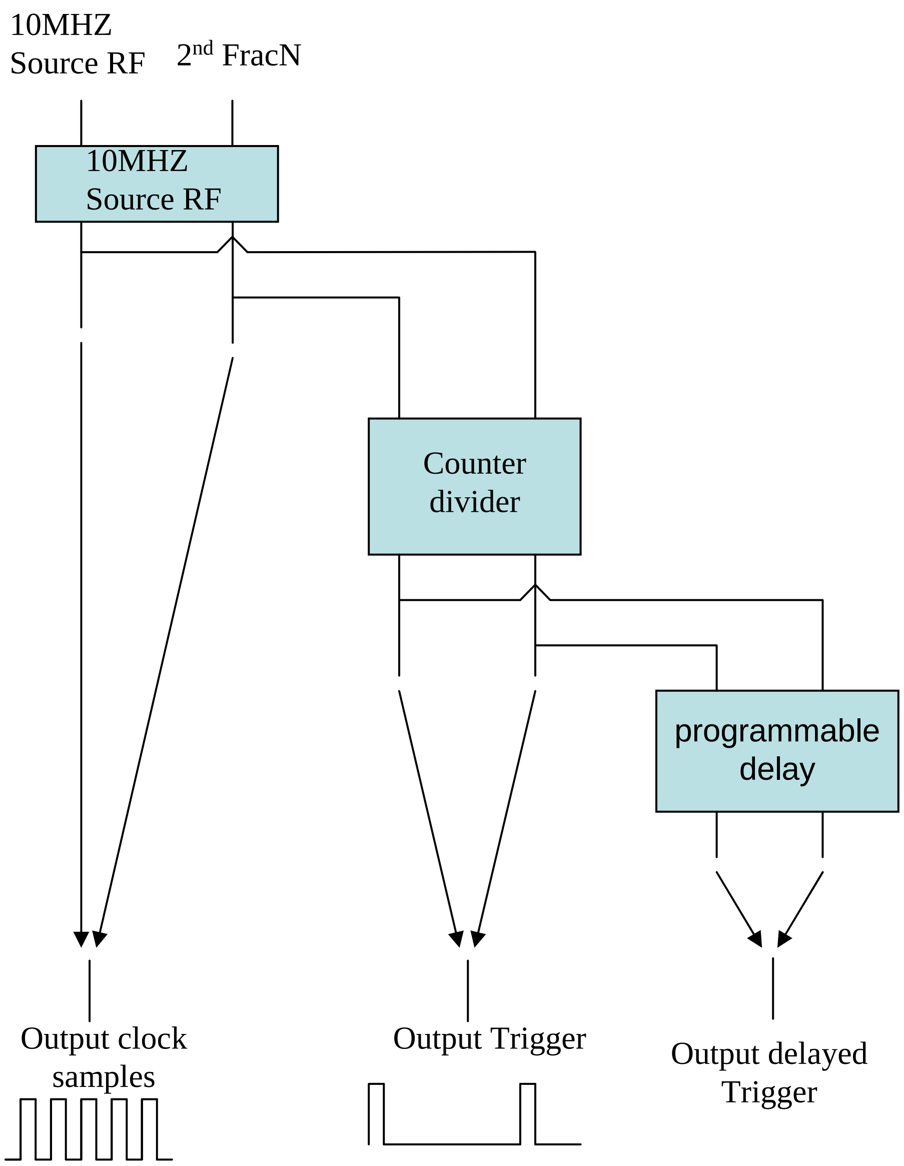
$$Fi0 = F0 - r0 \times Fsdc$$
$$\ldots$$
$$Fim = (m+1) \times F0 - rm \times Fsdc < Ffiltre$$
$$Fadc > 2 \times Fim$$

- Plus : Careful selection for the Pulse Period.
  Locking the phase of all signals on the reference signal(10 MHz).

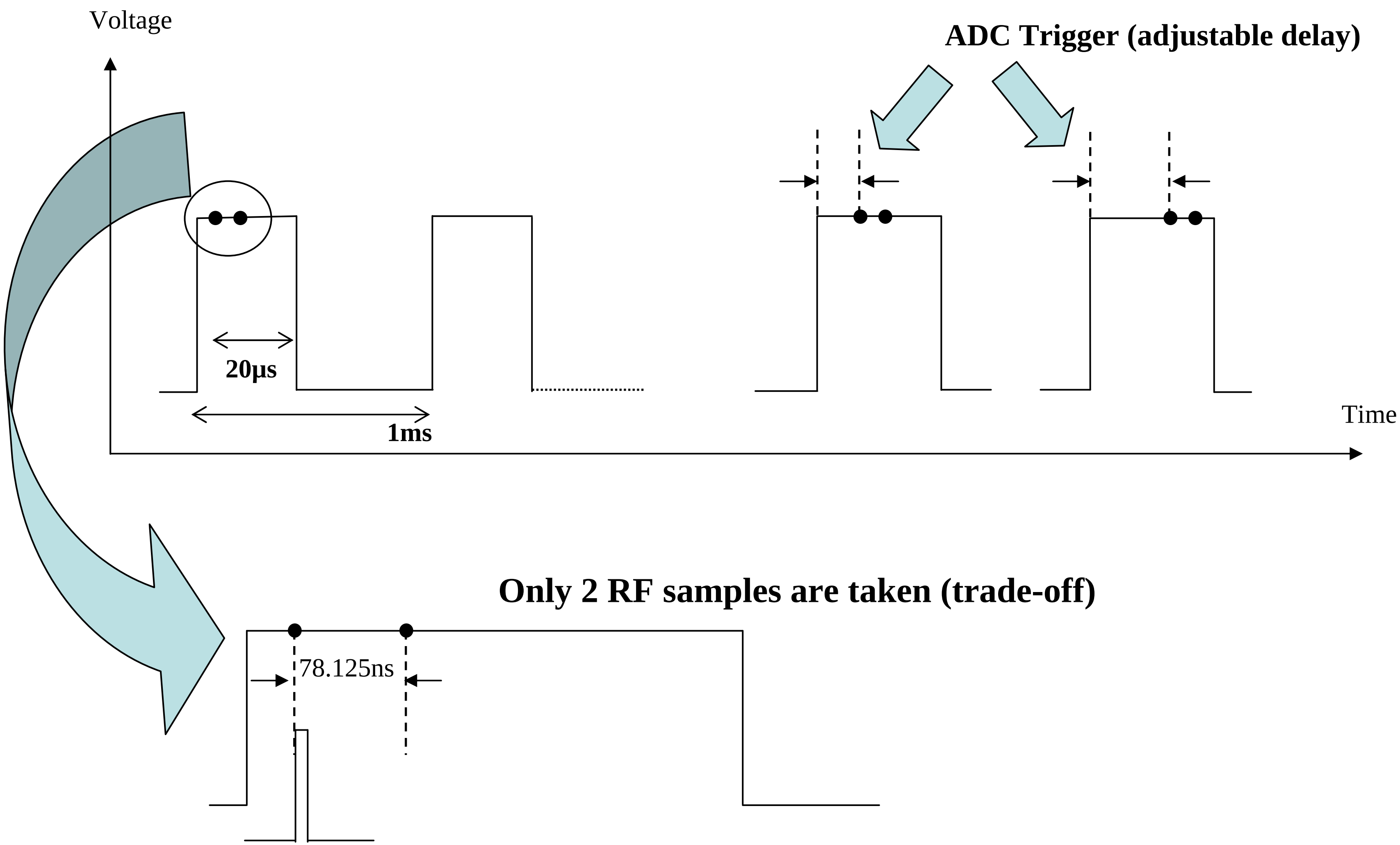
Development of a specific program

- *Input :F0, n, Ppa (arbitrary Pulse period)*
- *Output : Fi0, Fsdc, Fadc, Pc, r0, b0, m+1*

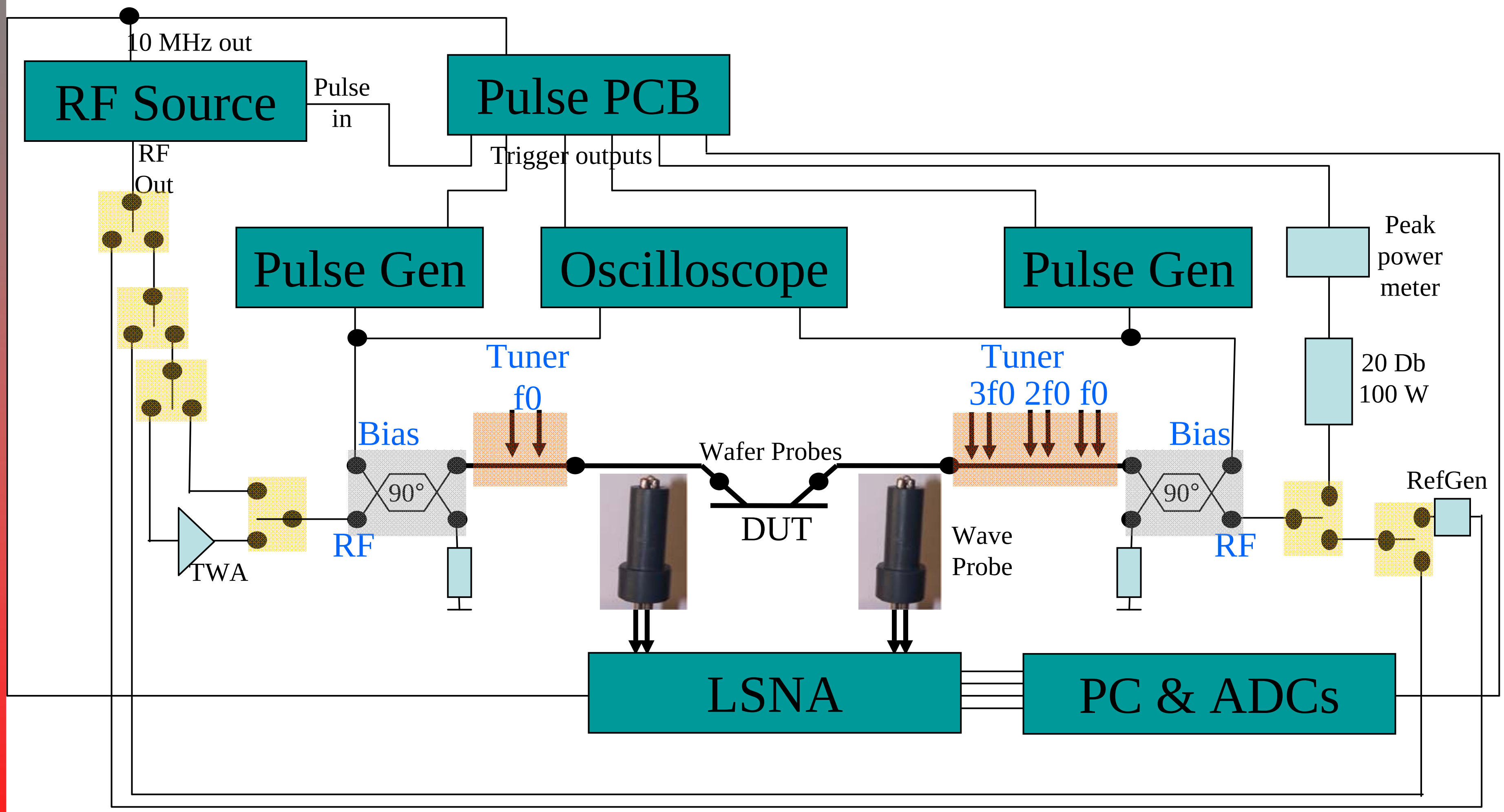
Clock generation for the pulse profiling mode



Adjustable Trigger Delay for Pulse Profiling



Bench structure for Load-Pull Pulse Profiling Mode



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Vgs0, Vds0 : bias point

Vgsi, Vdsi : a pulsed point

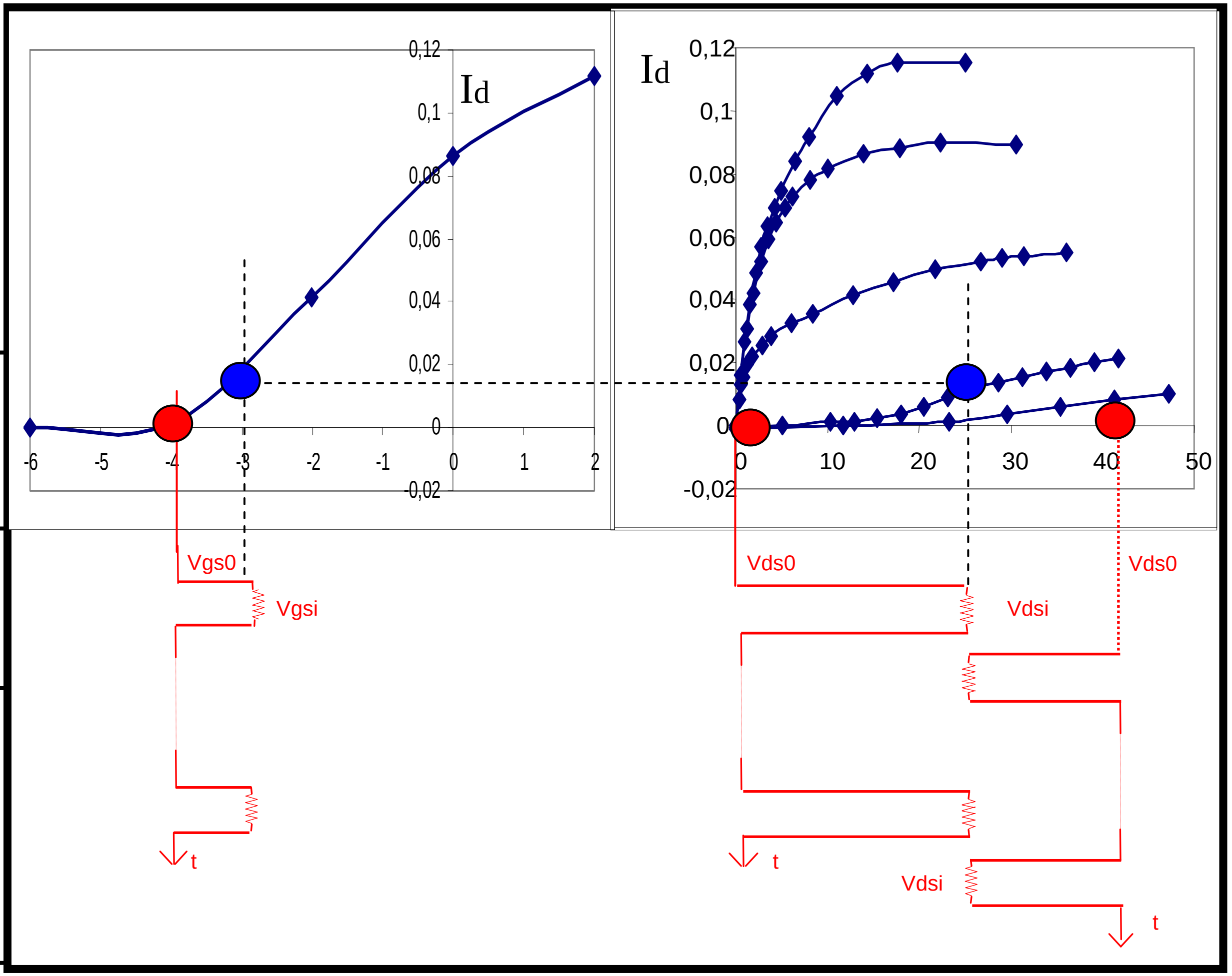
For our Measurements:

Vds0= 0V / 40V
Vgs0=-4.5V=Vp

Vdsi=25V
Vgsi=-3V

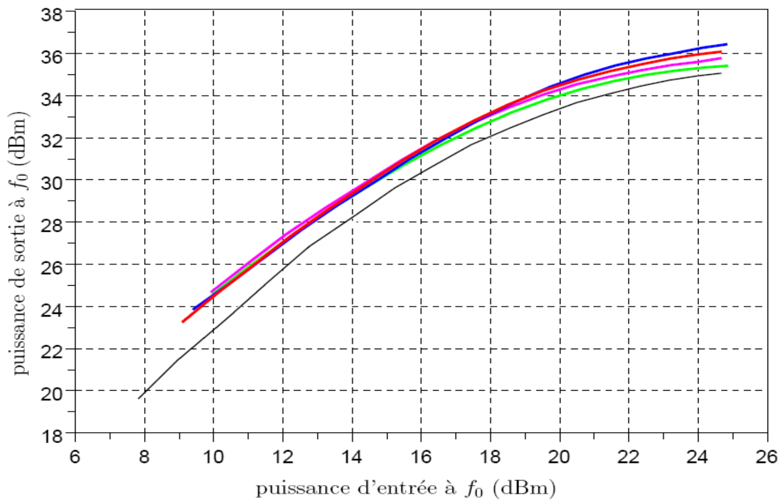
Pperiod =100 µs

Pwidth =10µs



The PIV controls the thermal and traps history

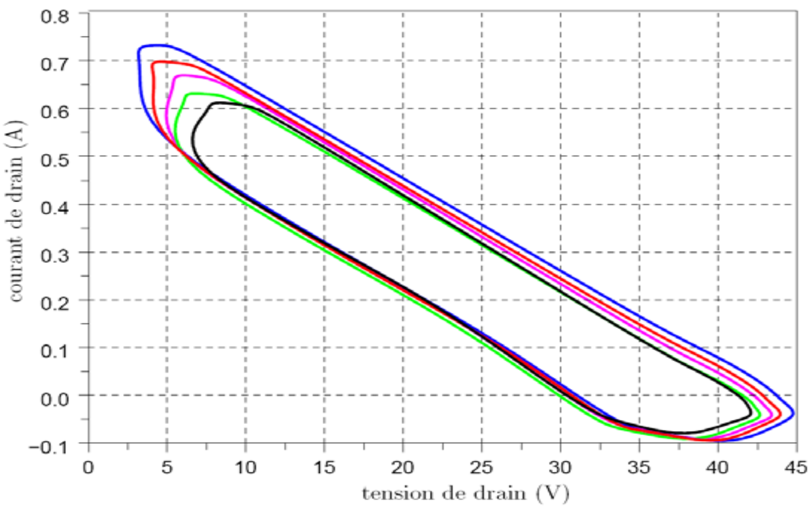
Output Power @f0 **for different polarizations of drain** (0-10-25-40V) with fixed gain compression (2dB)



Vdsi =25V for all the case

AB Polarization class

- **CW**
- **Pulsed 10µs-100µs Vds0 @ 0V**
- **Pulsed 10µs-100µs Vds0 @ 10V**
- **Pulsed 10µs-100µs Vds0 @ 25V**
- **Pulsed 10µs-100µs Vds0 @ 40V**



Cycles @f0 with one input power **for different Pulse biasing configuration** with a fixed gain compression (2dB) **and fixed delay**.

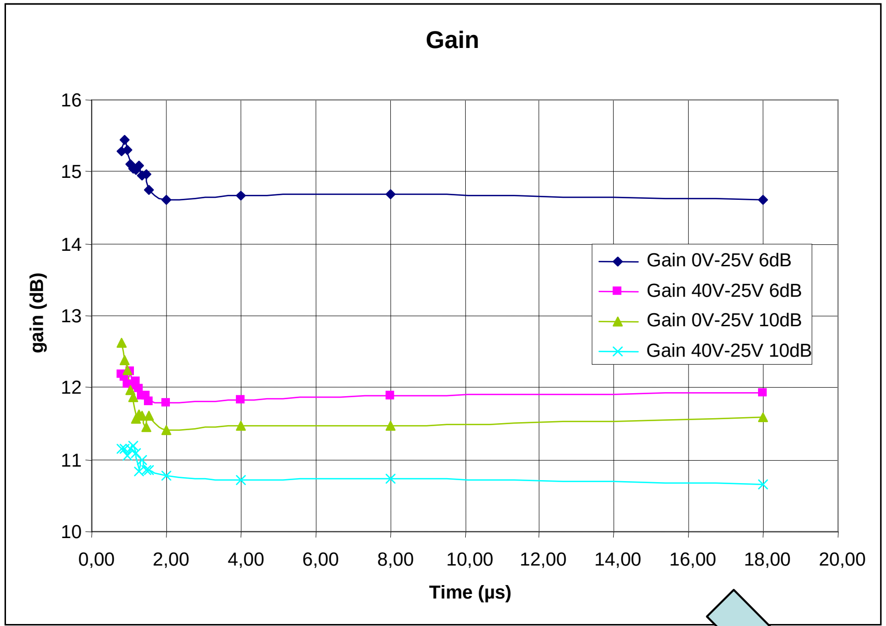
Gain and Phase @f0 for different PIV configuration

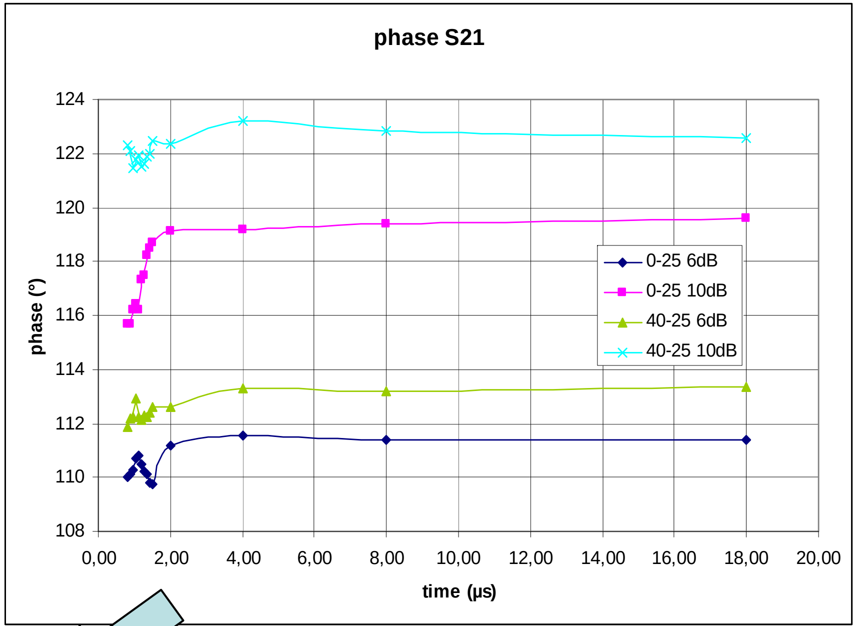
Vdsi=25V; Vds0=0V / 40V

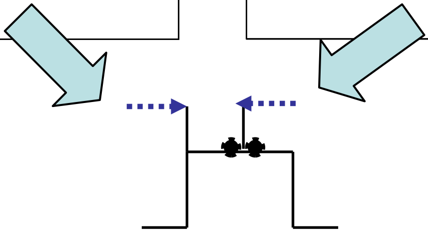
For 2 Input Power Levels and Gain Compression of 6dB and 10 dB

AlGaN/GaN HEMT from Alcatel-thales III-V Lab, 1 mm gate width

Vgs0=-4.5=Vp; Vgsi=-3V







Pulse profiling results: Power and Harmonics

Output Power @f0 and @2f0 for different PIV configuration

Vdsi=25V; Vds0=0V / 40V

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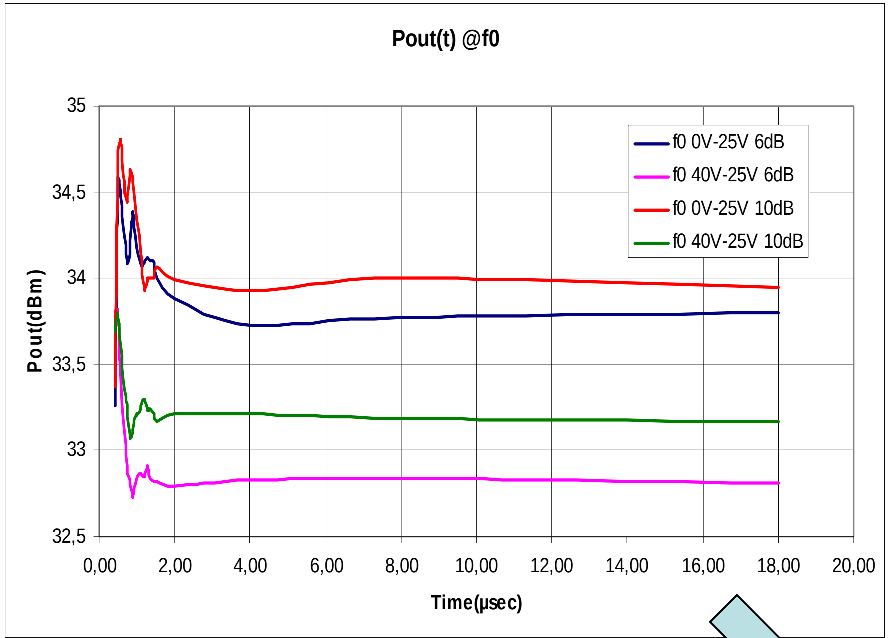

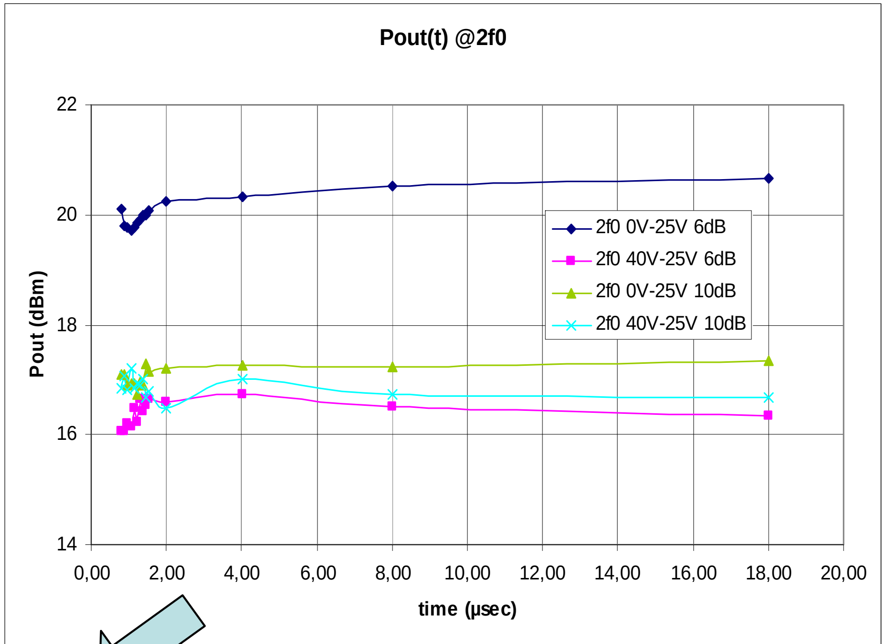

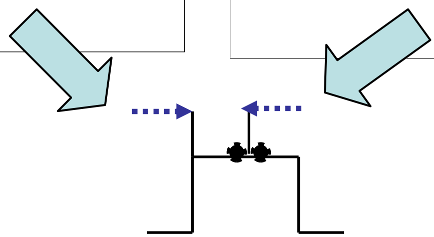

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Conclusion

- New capabilities for the characterization of nonlinear microwave active circuits.
- Helpful for memory investigations within devices
- View of system-level consequences of memory effects

Future Works

- This work will allow us to perform Pulse to Pulse or Bursts of Pulses Characterizations.

Thank you for your attention