Workshop on Advanced Measurements for RF Silicon

Organizers: Joe Gering, Qorvo, and Scott Parker, Qorvo

Time: Wednesday, January 29, 2020, 8:00 - 12:00

Abstract:
Bulk silicon and silicon-on-insulator (SOI) have long been a mainstay in digital and analog applications. These technologies also play a prominent role in RF, microwave, and millimeter-wave applications from radars to cellular phones. This joint workshop between ARFTG and SiRF will address some of the measurement challenges associated with RF silicon. It will start from a user's perspective with talks on the needs in modeling and with transceiver circuits. It will then shift to a measurement perspective with presentations on over-the-air (OTA), ESD, and calibration. Taken in entirety, this workshop will be an excellent resource for metrologists and RF designers alike.

Program:

7:55-8:00	Welcome
8:00-8:45	***The ABCs of RF Silicon Modeling for Measurement Engineers*** Scott Parker, Qorvo
8:45-9:30	***Characterization Challenges of Highly Integrated Transceivers for Radar and Communication Applications*** Vadim Issakov, University of Magdeburg, Germany
9:30-9:45	Break
9:45-10:30	***OTA Measurements of 5G and Millimeter-Wave Building Blocks*** Jon Martens, Anritsu
10:30-11:15	***High-Speed TLP and ESD Characterization of Silicon ICs*** Kathy Muhonen, Qorvo
11:15-12:00	***How to Design Your Own on-Wafer Calibration Standards and Why You Should Do It*** Andrej Rumiantsev, MPI corporation, and Marco Spirito, TU Delft

The ABCs of RF Silicon Modeling for Measurement Engineers

Scott Parker, Qorvo

Abstract: As the overall performance of CMOS and BiCMOS Technologies increases so too does their usage in RF applications that were formerly the sole domain of III-V technologies. Competitive RF performance combined with low cost (at high volume) and the ability to integrate digital control and die calibration on chip often give RF-CMOS based designs the win. As such, a CMOS modeling focus that was once aimed at logic gate timing, ring oscillator performance, and digital corner models is no longer sufficient. The RF-CMOS modeler now faces many of the same challenges faced by the III-V device modeler coupled with an increased palette of devices and the ever-present CMOS parasitics. This workshop presentation will cover some of the needs and challenges of RF-CMOS Modeling and thus RF-CMOS Characterization. It will focus on three, separate but closely related areas. First, it will give an overview of the various types of characterization a compact modeler needs on the active and passive devices in a typical RF-CMOS technology. Next, it will go into the measurement and modeling challenges associated with device, wiring, and substrate parasitics. Finally, it will cover the challenge of bridging the gap between wafer level measurements and the packaged die that designers are creating, and customers are buying.

Biography: Scott Parker is a Qorvo Senior Member of Technical Staff and Qorvo's lead for silicon modeling. He has been with Qorvo for 12 years and with IBM in Burlington Vermont for 23 years prior to that. Scott made the full progression from lab technician, to modeling engineer, and eventually to modeling manager at IBM responsible for low power bulk CMOS models at the 90nm, 65nm, and 45nm nodes. His focus since joining RFMD/Qorvo has been in supporting the modeling needs of designers across numerous BiCMOS, Bulk CMOS, and SOI CMOS platforms. Scott graduated from Vermont Technical College in 1984 with a A.S.E.E and The University of Vermont in 1994 with a B.S.E.E. He has three patents to his name and has been the author of numerous presentations on CMOS modeling at both IBM and RFMD/Qorvo.

Characterization Challenges of Highly Integrated Transceivers for Radar and Communication Applications

Vadim Issakov, University of Magdeburg, Germany

Abstract: Recent advances of silicon-based semiconductor processes and packaging technologies have accelerated the implementation of radar sensors for numerous mass-volume applications at mm-wave frequencies. CMOS and SiGe technologies seem to provide a very attractive solution for realization of mm-wave radar transceivers. However, with the advanced complexity of the transceivers also the complexity of the silicon verification is steadily increasing. This talk addresses the challenges of characterization of highly integrated chipsets in silicon-based technologies.

First, we discuss the increasing level of integration of radar and communication products towards System-on-Chip. Next, we discuss what key parameters must be characterized for RF systems. Then we discuss practical issues of measuring very complex chips on-wafer or on-PCB. Further, we discuss difficulties of de-embedding and interpreting the results at mm-wave frequencies. Next, we discuss particular challenges characterizing chips at mm-wave frequencies: such as e.g. uncertainty of input power to the DUT, very high ripple due to harmonic mixers, insufficient power to saturate the receiver, difficulty to measure the noise figure, repeatability of measurements. Finally, we show examples of measurements of 60GHz radar transceiver in CMOS and 120GHz radar transceiver in BiCMOS SiGe.

Biography: Vadim Issakov received the M.Sc. degree in microwave engineering from the TU Munich in 2006 and the Ph.D. degree from the University of Paderborn, Germany, in 2010.

In March 2010 he joined Infineon in Neubiberg, Germany. Afterwards he worked at IMEC and Intel Corporation, before he came back to Infineon in August 2015 as mm-wave Design Lead and Principal Engineer leading a research group working on pre-development of mm-wave radar and communication products. In September 2019 he joined the University of Magdeburg, Germany, as a full professor holding the Chair for Electronics. His research interests include mm-wave circuits, RF systems, mm-wave measurement techniques and RF-ESD.

His work has been recognized by the IEEE MTT Outstanding Young Engineer Award 2019.

OTA Measurements of 5G and Millimeter-Wave Building Blocks

Jon Martens, Anritsu

Abstract: Integrated radio and subsystem designs are increasingly common and OTA measurements are often needed. When that testing is at the parametric level, there can be a number of challenges in calibration and analysis for both linear and quasi-linear quantities. Approaches for measurements ranging from simpler elemental phase analysis (with or without frequency conversion) to distortion metrics will be explored with an emphasis on sensitivities and potential problem areas.

Biography: Jon Martens has been with Anritsu since 1995 working on measurement system architectures and mm-wave circuit/subsystem design. He is a past president of the measurement society ARFTG and a former associate editor of the IEEE Transactions on Microwave Theory and Techniques.

High-Speed TLP and ESD Characterization of Silicon ICs

Kathy Muhonen, Qorvo

Abstract: Electrostatic discharge is always an area of concern in reliability and production of ICs. In order to design effective ESD clamps, knowing how the clamp turns on and operates during an ESD event is critical. This cannot be done with S-parameters or any other type of typical RF characterization. Transmission Line Pulsing, TLP, is a high-speed system that mimics an ESD event with a very short flat pulse (<100nsec is typical). This allows in situ measurement of the voltage and current at the DUT during an ESD-like event. This workshop presentation will give an introduction into the theory (which is based on time domain reflection), configuration and uses of TLP. Different TLP configurations will be reviewed and all will extract an IV curve for the DUT response. Calibration and correction will be explained which are done in the time domain. These provide the voltage and current references. The importance of the TLP load line will be discussed and its application to DUT characterization of turn-on and snap-back. Finally, the newest characterization, Very Fast TLP, will be presented and its hurdles to accurate calibration.

Biography: Kathleen Muhonen is currently an ESD Design Engineer at Qorvo. She is involved in ESD on-chip protection for RF applications. She is also involved standardizing the testing of RF components for ESD. Previously she was responsible for characterization and model support for SOI and GaAs. This included work on developing on-wafer harmonic characterization of semiconductors and improving de-embedding techniques of large-scale switches. Kathleen's previous experience includes assistant professor at Penn State Erie, power amplifier designer at Hewlett Packard, Lockheed Martin and GE Aerospace. Kathleen is member of the ESD Association device testing standards development, including serving as a workgroup chair and Board of Directors. She has generated several key papers to help standardization of ESD testing over the last decade. She received a BSEE from Michigan Tech in 91, an MSEE from Syracuse in 94, and a Ph.D.EE from Penn State in 99.

How to Design Your Own on-Wafer Calibration Standards and Why You Should Do It

Andrej Rumiantsev, MPI corporation, and Marco Spirito, TU Delft

Abstract: Wafer-level S-parameter measurement at mm-wave and sub-mm wave frequencies plays a crucial role in the model development and IC design verification of advanced semiconductor technologies. Accurate calibration of the entire wafer-level measurement system to the RF probe tip end or to the intrinsic device terminals is a critical success factor for extracting trustable device model parameters and characterizing true performance of a RF IC. Challenges of obtaining accurate, reproducible and trustable results drastically increase with the frequency: methods and practices that have been working well, tend to fail or to yield results which are difficult to interpret. In particular, this concerns de-embedding of the device back end of line (BEOL) parasitics.

This talk will discuss the technique of on-wafer S-parameters calibration and why it is beneficial over the conventional probe-tip calibration methods for advanced silicon processes at the mm-wave and sub-mm wave frequencies. The on-wafer calibration shifts the measurement reference plane close to the device terminals in one step and thus removes the majority of the device BEOL infrastructure parasitics. We will review selection criteria of suitable calibration methods and the design of the required custom calibration standards. The presented approach significantly improves the accuracy of device characterization, in particular, at sub-mm wave frequencies and simplifies the de-embedding of the device parasitics when it is still required.

Biography: Andrej Rumiantsev received the Diploma-Engineer degree (with highest honors) in Telecommunication systems from the Belarusian State University of Informatics and Radio Electronics (BSUIR), Minsk, Belarus, and the Dr.-Ing. Degree (with summa cum laude) in Electrical Engineering from Brandenburg University of Technology (BTU) Cottbus, Germany, in 1994 and 2014, respectively. He joint SUSS MicroTec Test Systems (later Cascade Microtech) in 2001, where he held various engineering product management and marketing positions. In March 2013, he joined Ulrich L. Rohde Chair for RF and Microwave Techniques at Brandenburg University of Technologies (BTU), Cottbus, Germany. Dr. Rumiantsev is currently with MPI Corporation, holding a position of Director of RF Technologies of the Advanced Semiconductor Test Division. His research interests include RF calibration and wafer-level measurement techniques for advanced semiconductor devices, and he holds multiple patents in the area of wafer-level RF calibration and measurements techniques.

Dr. Rumiantsev is a member of the IEEE MTT-11 Microwave Measurements Committee and an ExCom member of ARFTG. He is a past ExCom member of IEEE BCTM, TPC member of BCICTS, past TPC Chair of ARFTG-92nd and ARFTG-93rd and the General Chair of ARFTG-94th. Dr. Rumiantsev received the ARFTG-71st Best Interactive Forum Paper Award, and his doctoral thesis was awarded "Best Dissertation of 2014 at Brandenburg University of Technologies".

Marco Spirito received his M.Sc. degree (cum laude) in electrical engineering from the University of Naples "Federico II," Naples, Italy, in 2000, and the Ph.D. degree from TU Delft in 2006. In 2008 he joined the Electronics Research Laboratory in TU Delft where he is an Associate Professor since 2013. In 2010 and 2017 he was one of the co-founders of Anteverta-MW and Vertigo Technologies, respectively, two companies pioneering innovative measurement techniques and hardware solutions.

Dr. Spirito was the recipient of the Best Student Paper Award for his contribution to the 2002 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM). He received the IEEE MTT Society Microwave Prize in 2008, was a co-recipient of the best student paper award at IEEE RFIC 2011, the GAAS Association Student Fellowship in 2012, best student paper award in second place at the IMBioC 2018, best paper at the 2019 Winter ARFTG Conference, and the best student paper award at the 2019 Summer ARFTG Conference.